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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,144	WORRELL, FRANK	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2001 and 29 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *2, 4-6, and 8-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-14 have been examined.

Papers Received

2. Receipt is acknowledged of change of address paper submitted, where the paper has been placed of record in the file.

Drawings

3. The drawings are objected to because in figures 1 and 2 it is unclear what element 100 is pointing to. The examiner suggests that if the intent is to point to the entire system shown that the applicant simply draw a box around the system and have the indicator point to the box. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: The headings of each section should not be underlined or in boldface type as described in 37 CFR 1.77(c).

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Predict Taken Algorithm that Waits for Evaluation of the Condition Before Prefetching the Next Instruction.

Appropriate correction is required.

Claim Objections

6. Claim 2 is objected to because of the following informalities:

a. It is unclear what the prefetching function of mention is. If the condition of the branch has already been evaluated and thus the branch has been executed, a pipeline would then be ready for the next instruction. This would simply mean fetching as opposed to prefetching since the address will be presented when needed and not ahead of time. The examiner requests clarification on this matter.

b. The claim does not show any relationship between the sequential instruction address and the branch target address as described in the specification where the sequential instruction address is for the instruction following the target address.

7. Claim 4 is objected to because of the following informalities: the claim recites the limitation "a second predetermined offset" in line 4. There is no first predetermined offset. The only other offset of mention is in claim 3 and cannot be related to the offset of claim 4 because claim 4 does not depend on claim 3. The term "second" could also simply be the name of the offset, however, the examiner is taking the phrase "a second predetermined offset" to mean "a predetermined offset."

8. Claim 5 is objected to because of the following informalities: the claim states "an address displacement of said branch condition." The meaning of this phrase is unclear. The examiner is taking it to mean "an address displacement of said branch instruction."

9. Claim 6 is objected to because of the following in formalities:

a. The claim does not show any relationship between the sequential instruction address and the branch target address as described in the specification where the sequential instruction address is for the instruction following the target address.

b. Lines 8-9 of the claim make use of "a program counter address" when a program counter address has already been defined. It is unclear whether there is a correlation between the separately mentioned program counters or not. The examiner is taking the phrase to mean "the program counter address" an thus to mean the same program counter address previously mentioned in the claim in order to give the claim the broadest reasonable interpretation and to stay consistent with claim 13.

c. The claim states "an address displacement of said branch condition." The meaning of this phrase is unclear. The examiner is taking it to mean "an address displacement of said branch instruction."

d. It is unclear what the prefetching function of mention is. If the condition of the branch has already been evaluated and thus the branch has been executed, a pipeline would then be ready for the next instruction. This would simply mean fetching as opposed to prefetching since the address will be presented when needed and not ahead of time. The examiner requests clarification on this matter.

10. Claim 8 is objected to because of the following informalities: The claim does not show any relationship between the sequential instruction address and the branch target

address as described in the specification where the sequential instruction address is for the instruction following the target address.

11. Claims 9-13 are objected to because of the following informalities: It is unclear whether the claims are further limiting the circuit mentioned in claim 7 or simply the microprocessor in general.

12. Claim 9 is objected to because of the following informalities: Claim 7 states that the branch target address and the mispredict recovery address are the inputs to the multiplexer. This means that one of these signals will be the output of the multiplexer. Claim 9 gives a different name to this output, a program counter address. It is requested that a correlation between the selection of the mispredict recovery address or the branch target address and the program counter address be shown if one indeed exists.

13. Claim 10 is objected to because of the following informalities:

a. Claim 7 states that the branch target address and the mispredict recovery address are the inputs to the multiplexer. This means that one of these signals will be the output of the multiplexer. Claim 9 gives a different name to this output, a program counter address. It is requested that a correlation between the selection of the mispredict recovery address or the branch target address and the program counter address be shown if one indeed exists.

b. The claim says that a program counter address is presented by said multiplexer and used in generating said branch target address, however, claim 7, says that the multiplexer receives the branch target address. It is unclear how

the multiplexer can send information to generate the branch target address when it is receiving this signal.

14. Claim 13 is objected to because of the following informalities:

a. Claim 7 states that the branch target address and the mispredict recovery address are the inputs to the multiplexer. This means that one of these signals will be the output of the multiplexer. Claim 9 gives a different name to this output, a program counter address. It is requested that a correlation between the selection of the mispredict recovery address or the branch target address and the program counter address be shown if one indeed exists.

b. The claim says that a program counter address is presented by said multiplexer and used in generating said sequential instruction address and said branch target address, however, claim 7, says that the multiplexer receives the branch target address and claim 13 has previously said that the multiplexer also receives the sequential instruction address. It is unclear how the multiplexer can send information to generate the branch target address and sequential instruction address when it is receiving these signals.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

15. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

16. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

17. Claim 9 recites the limitation "said sequential instruction address" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim. Claim 7, the parent claim, does not make any mention of a sequential instruction address. The examiner will take the claim to mean "a sequential instruction address."

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claims 1-2, 7-8, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Moyer (5,951,678).

20. In regard to claim 1, Moyer discloses a method of conditional branching in a pipelined processor (figure 1), the method comprising the steps of:

a. prefetching a branch target address in response to encountering a branch instruction, in prediction of taking a branch; In column 6, lines 33-37, Moyer discloses a mode where he prefetches the destination address of the branch and uses a predict taken algorithm.

b. evaluating between taking said branch and not taking said branch substantially contemporaneously with prefetching said branch target address. In

figure 4, Moyer has shown where the destination (target) is being prefetched while the condition is being evaluated. Instruction Q is a conditional branch and instruction S is the target (column 4, lines 48-50). When the instruction Q is in the decode stage as shown, the branch instruction and its condition is realized. The condition is then evaluated and eventually resolved at the end of the cycle as indicated in the figure and in column 4, lines 54-56. The target, S, is fetched (or prefetched as indicated by the title of the figure) while the condition is being evaluated as shown in the figure.

21. In regard to claim 2, Moyer discloses the method of claim 1, as described above, further comprising the steps of: prefetching a sequential instruction address in response to evaluating to take said branch; or prefetching a mispredict recovery address in response to evaluating not taken said branch. In column 4, lines 36-38, Moyer discloses that once the condition is resolved (branch has been evaluated), the appropriate instruction can then be fetched. This instruction inherently is the sequential instruction at the branch target or the recovery instruction, which is the instruction immediately following the initial branch instruction.

22. In regard to claim 7, Moyer discloses a pipelined processor (figure 1) comprising:

A multiplexer (figure 1, element 24); and

A circuit (figure 1) configured to present

i. A branch target address to said multiplexer in prediction of taking a branch; The branch target address is presented by the execution unit

(element 40), because it needs to be calculated, as the operand address to the multiplexer (element 24).

ii. A mispredict recovery address to said multiplexer when not taking said branch. The mispredict recovery address is presented by the program counter calculator (element 28), which increments the address, to the multiplexer (element 24) as the instruction address.

23. In regard to claim 8, Moyer discloses the pipelined processor of claim 7, as described above, wherein said circuit (figure 1) is further configured to present a sequential instruction address to said multiplexer (figure 1, element 24) when taking said branch. The circuit of figure 1 presents the sequential address as the instruction address through the program counter calculator when the branch is taken. This instruction address is presented to the multiplexer (element 24).

24. In regard to claim 14, Moyer discloses a pipelined processor comprising:

a. A means for multiplexing (figure 1, element 24);

b. A means for presenting a branch target address to said means for multiplexing in prediction of taking a branch; The branch target address is presented by the execution unit (element 40), because it needs to be calculated, as the operand address to the means for multiplexing.

c. A means for presenting a mispredict recovery address to said means for multiplexing when not taking said branch. The mispredict recovery address is presented by the program counter calculator, which increments the address, to the means for multiplexing as the instruction address.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 3-6, 9-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Hennessy.

27. In regard to claim 3, Moyer discloses the method of claim 2, as described above, further comprising the step of:

a. generating said sequential instruction address; Moyer also discloses the existence of a program counter and that calculations can be performed on it in figure 1, element 28, program counter calculator.

b. Moyer does not disclose that the sequential instruction address is generated based upon a program counter address and a predetermined offset.

c. Hennessy has taught on page 404, top paragraph, that a sequential PC is always computed for every instruction. On the table directly below, Hennessy has taught that the sequential instruction address is generated using two source operands, the PC (program counter) and the number 4 (a predetermined offset).

d. By always computing the sequential address from the target address in the program counter using the method described by Hennessy, a uniform and simple method of sending control to the next instruction is established. This uniformity and simplicity would have motivated one of ordinary skill in the art to

modify Moyer's design to incorporate the method of generating sequential addresses given by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer to include the sequential addressing method of Hennessy in order to have a uniform and simplistic design.

28. In regard to claim 4, Moyer discloses the method of claim 2, as described above, further comprising the step of:

a. generating said misprediction recovery address; Moyer also discloses the existence of a program counter and that calculations can be performed on it in figure 1, element 28, program counter calculator.

b. Moyer does not disclose that the misprediction recovery is generated based upon a program counter address and a predetermined offset.

c. Hennessy has taught on page 404, top paragraph, that a sequential PC is always computed for every instruction. The mispredict recovery address is simply a sequential address from the branch instruction address. On the table directly below, Hennessy has taught that the sequential instruction address is generated using two source operands, the PC (program counter) and the number 4 (a predetermined offset).

d. By always computing the sequential address from the branch instruction address in the PC using the method described by Hennessy, a uniform and simple method of sending control to the next instruction is established. This uniformity and simplicity would have motivated one of ordinary skill in the art to

modify Moyer's design to incorporate the method of generating sequential addresses given by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer to include the sequential addressing method of Hennessy in order to have a uniform and simplistic design.

29. In regard to claim 5, Moyer discloses the method of claim 1, as described above, further comprising the step of:

a. generating said branch target address; The fact that Moyer has branch target addresses means that they must be generated. Moyer also discloses the existence of a program counter as shown by his program counter calculator in figure 1.

b. Moyer does not disclose that this branch target address is based upon a program counter address and an address displacement of said branch instruction.

c. Hennessy, on page 148 discloses the use of an offset or displacement to be added to some position stored in a register, which yields a branch target address. The program counter given by Moyer is a register because it holds a value.

d. Hennessy discloses that using his method to calculate the branch target address provides a large range of possible targets for the branch. Hennessy also teaches on last paragraph that by using the PC as the register, hardware convenience is established. This large range of addressing possibilities and

hardware convenience would have motivate done of ordinary skill in the art to implement the method of Hennessy in Moyer for greater address range and hardware convenience.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Moyer's invention to generat the branch target address based upon a program counter address and an address displacement of the branch instruction as taught by Hennessy in order to have a wide range of addresses to branch to and for hardware convenience.

30. In regard to claim 6, Moyer discloses the method of claim 1, as described above, further comprising the steps of:

a. generating said sequential instruction address based upon a program counter address and a predetermined offset as described above in paragraph 27.

b. generating said misprediction recovery address based upon an exception program counter address and a predetermined offset as seen above in paragraph 28.

c. Generating said branch target address based upon a program counter address and an address displacement of said branch instruction as seen above in paragraph 29.

d. prefetching a sequential instruction address in response to evaluating to take said branch; or prefetching a mispredict recovery address in response to evaluating not taken said branch. In column 4, lines 36-38, Moyer discloses that once the condition is resolved (branch has been evaluated), the appropriate

instruction can then be fetched. This instruction inherently is the sequential instruction at the branch target or the recovery instruction, which is the instruction immediately following the initial branch instruction.

31. In regard to claim 9, Moyer discloses the pipelined processor of claim 7, as described above, further comprising:

a. a prefetch program counter (figure 1, included in element 28) for storing a program counter address presented by said multiplexer (figure 1, element 24). As shown in figure 1, the program counter address given by the program counter calculator (element 28) passes through the multiplexer (element 24) where it can then be passed back to the program counter calculator for storage. Moyer also must generate sequential instruction addresses;

b. Moyer does not disclose that the sequential instruction address is generated based upon a program counter address.

c. Hennessy has taught on page 404, top paragraph, that a sequential PC is always computed for every instruction. On the table directly below, Hennessy has taught that the sequential instruction address is generated using two source operands, one of which is the PC (program counter).

d. By always computing the sequential address from the target address in the program counter using the method described by Hennessy, a uniform and simple method of sending control to the next instruction is established. This uniformity and simplicity would have motivated one of ordinary skill in the art to

modify Moyer's design to incorporate the method of generating sequential addresses given by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer to include the sequential addressing method of Hennessy in order to have a uniform and simplistic design.

32. In regard to claim 10, Moyer discloses the pipelined processor of claim 7, as described above, further comprising:

a. a prefetch program counter (figure 1, included in element 28) for storing a program counter address presented by said multiplexer (figure 1, element 24). As shown in figure 1, the program counter address given by the program counter calculator (element 28) passes through the multiplexer (element 24) where it can then be passed back to the program counter calculator for storage. Moyer also must generate sequential instruction addresses; Moyer also discloses an instruction register (figure 1, element 30) for storing said branch instruction used in generating said branch target address. This register holds all instructions before execution and thus stores branch instructions, which have branch target addresses as described above.

b. Moyer does not disclose that the sequential instruction address is generated based upon a program counter address.

c. Hennessy has taught on page 404, top paragraph, that a sequential PC is always computed for every instruction. On the table directly below, Hennessy

has taught that the sequential instruction address is generated using two source operands, one of which is the PC (program counter).

d. By always computing the sequential address from the target address in the program counter using the method described by Hennessy, a uniform and simple method of sending control to the next instruction is established. This uniformity and simplicity would have motivated one of ordinary skill in the art to modify Moyer's design to incorporate the method of generating sequential addresses given by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer to include the sequential addressing method of Hennessy in order to have a uniform and simplistic design.

33. In regard to claim 12, Moyer discloses the pipelined process of claim 7, as described above, further comprising:

a. generating said misprediction recovery address; Moyer also discloses the existence of a program counter and that calculations can be performed on it in figure 1, element 28, program counter calculator.

b. Moyer does not disclose that the misprediction recovery is generated based upon a program counter address disposed in a decode stage.

c. Hennessy has taught on page 404, top paragraph, that a sequential PC is always computed for every instruction. The mispredict recovery address is simply a sequential address from the branch instruction address. On the table directly below, Hennessy has taught that the sequential instruction address is

generated using two source operands, one being the PC (program counter). Hennessy shows on page 506 the use of an exception program counter (EPC) disposed in the execute stage of the pipelined processor.

d. By always computing the sequential address from the branch instruction address in the PC using the method described by Hennessy, a uniform and simple method of sending control to the next instruction is established. Hennessy teaches on page 509 that the exception (a mispredicted branch in this case) is detected in the decode stage and handled in the execute stage. By handling it in the next clock cycle, one can be assured that the correct information will be present. This uniformity and simplicity coupled with integrity of data would have motivated one of ordinary skill in the art to modify Moyer's design to incorporate the method of generating misprediction recovery address given by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer to include the sequential addressing method of Hennessy in order to have a uniform and simplistic design with a high integrity of data while generating a misprediction recovery address.

34. In regard to claim 13, Moyer discloses the pipelined processor of claim 7, as described above, further comprising:

a. Said circuit being further configured to provide a sequential instruction address to said multiplexer for use upon choosing to take said branch as described above in paragraph 23;

b. a prefetch program counter for storing a program counter address presented by said multiplexer and used in generating said sequential instruction address and said branch target address as described above in paragraph 31;

c. an instruction register (figure 1, element 30) for storing said branch instruction used in generating said branch target address as described above in paragraph 32;

d. Moyer discloses:

i. generating said misprediction recovery address; Moyer also discloses the existence of a program counter and that calculations can be performed on it in figure 1, element 28, program counter calculator.

ii. Moyer does not disclose that the misprediction recovery is generated based upon a program counter address.

iii. Hennessy has taught on page 404, top paragraph, that a sequential PC is always computed for every instruction. The mispredict recovery address is simply a sequential address from the branch instruction address. On the table directly below, Hennessy has taught that the sequential instruction address is generated using two source operands; one is the PC (program counter).

iv. By always computing the sequential address from the branch instruction address in the PC using the method described by Hennessy, a uniform and simple method of sending control to the next instruction is established. This uniformity and simplicity would have motivated one of

ordinary skill in the art to modify Moyer's design to incorporate the method of generating sequential addresses given by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Moyer to include the sequential addressing method of Hennessy in order to have a uniform and simplistic design.

35. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Hennessy, as applied above to claim 12, in further view of Eckner (6,044,460).

36. In regard to claim 11, Moyer in view of Hennessy discloses the pipelined process of claim 7, as described above, further comprising:

a. An exception program counter for storing an exception program counter address used in generating said misprediction recovery address;

b. Moyer in view of Hennessy does not disclose that the program counter is disposed in a decode stage.

c. Eckner shows in figure 3 the use of an exception program counter disposed in the decode stage (element 408) of the pipelined processor. Column 6, line 66 – column 7, line 1 states the explicit coupling of the EPC in the decode stage.

d. The exception program counter placement taught by Eckner allows for the use of the handling of an exception as soon as possible. This means that fewer pipeline cycles need to be flushed than if the exception program counter was placed later in the pipeline. This advantage of time saved would have motivated

one of ordinary skill in the art to modify Moyer's design to incorporate the placement of the exception program counter as described by Eckner.

It would have been obvious to one of ordinary skill in the art at the time of invention to assure that Moyer placed the exception program counter in the decode stage as taught by Eckner so that the fewer pipeline stages need to be flushed and time is saved.

Conclusion

37. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to conditional branching in general.

US Pat No 6,088,793 to Liu shows a method for fetching instructions after encountering a branch instruction.

US Pat No 6,493,821 to D'Sa gives a method for branch misprediction recovery.

US Pat No 6,330,664 to Halvarsson teaches the use of conditional jumps and their target addresses and prefetching instructions after the jumps.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
September 23, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100